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EXAMINER

NGUYEN, CUONG QUANG

ART UNIT PAPER NUMBER

2811

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No. 10/694,675	Applicant(s) RIGHTER, ALAN W.	
	Examiner Cuong Q. Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 and 45-50 is/are pending in the application.
- 4a) Of the above claim(s) 26,31 and 48-50 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-32 and 45-47 is/are rejected.
- 7) ☒ Claim(s) 10 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>04-25-05</u> | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Embodiment I, claims 1-25, 27-30, 32 and 45-47 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-8, 11-12, 16-19, 21, 27-30, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Nojiri (US 2001/0045670 A1).

Regarding claims 1, 2, 4, 11, 12, 28, 29, 32, Nojiri discloses a bond pad structure for an EDS integrated circuit, comprising: a first active device (a plurality of PMOS P1) and a second active device (a plurality of NMOS N1) formed in a substrate; a first bus (a power supply line VDD) and a second bus (a power return line VSS) above the first and

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second active devices, respectively; a bond pad (28) above the first and second buses; first interconnections between the first and second active devices and the bond pad; and second interconnections between the first and second active devices and the first and second buses, respectively. See Nojiri's Fig.6-7.

Regarding claims 3, 30, as shown in Nojiri's Fig.1-2, PMOS and NMOS transistors each include two or more connected source fingers, two or more connected drain fingers and two or more connected gate fingers which are elongated in a direction of current flow in the first and second buses and which are narrow perpendicular to the direction of current flow.

Regarding claim 5, as shown in nojiri's Fig.6-7, first and second buses connect to a plurality of bond pad structures on an integrated circuit chip.

Regarding claims 7, 8, as shown in nojiri's Fig.6-7, conductive islands are formed in the first and second buses for connection of the bond pad to the PMOS and NMOS transistors.

Regarding claim 16, as shown in nojiri's Fig.6-7, the PMOS and NMOS transistors are interconnected in a CMOS configuration.

Regarding claim 17, as shown in nojiri's Fig.6-7, a metal level for connections to the gates of the PMOS and NMOS transistors.

Regarding claim 18, as shown in nojiri's Fig.6-7, the t interconnections comprise connections between the bond pad and the drains of the PMOS and NMOS transistors.

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Regarding claim 19, as shown in nojiri's Fig.6-7, the second interconnections comprise a connection between the power supply bus (VDD) and the source (9) of the PMOS transistor.

Regarding claim 21, as shown in nojiri's Fig.6-7, the second interconnections comprise a connection between the power return bus (VSS) and the source (7) of the NMOS transistor.

Regarding claim 27, as shown in nojiri's Fig.6-7, the bonding pad comprises a single relative thick layer (16).

Claims 1, 2, 4, 11, 13-15, 28-29, and 45-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (6,788,507).

Regarding claims 1, 2, 4, 11, 28, 29, Chen et al. discloses a bond pad structure for an EDS integrated circuit, comprising: a first active device (a PMOS 110) and a second active device (a NMOS 140) formed in a substrate; a first bus (a power supply line VDD) and a second bus (a power return line VSS) above the first and second active devices, respectively; a bond pad (92 I/O pad) above the first and second buses; first interconnections between the first and second active devices and the bond pad; and second interconnections between the first and second active devices and the first and second buses, respectively. See Chen et al.'s Fig.2-4.

Regarding claims 13-15, 45-47, as shown in Chen et al.'s Fig.3, a guard band region formed in the substrate, wherein the guard band region comprises an N+ guard

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band (118) in an N-well (120) for isolation of the PMOS transistor, a P+ guard band (148) for isolation of the NMOS transistor and conductive interconnects between the power supply bus and the N+ guard band and between the power return bus and the P+ guard band, wherein in the N+ guard band surrounds the PMOS transistor and the P+ guard band surrounds the NMOS transistor.

Claims 1 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ebara (US 6,858,885).

Regarding claim 1, Nojiri discloses a bond pad structure for an EDS integrated circuit, comprising: a first active and a second active device formed in a substrate; a first bus (a power supply line bus 13a) and a second bus (a power return line bus 13b) above the first and second active devices, respectively; a bond pad above the first and second buses; first interconnections between the first and second active devices and the bond pad; and second interconnections between the first and second active devices and the first and second buses, respectively. See Ebara's Fig.1A-1B.

Regarding claim 24, as shown in Ebara's Fig.1A-1B, the bond includes two or more space-apart bond pad layers (25c, 13c, 7). And wherein the two or more bond pad layers are interconnected by a plurality of individual contacts within a passivation opening associated with the bond pad structure.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9, 20, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nojiri in view of Brintzinger (US 6,495,918).

Nojiri teaches all the limitations of claims 1-5, 7-8, 11-12, 16-19, 21, 27-30, and 32 as shown above but does not teach that each of the interconnections comprises a plurality of individual lines.

Brintzinger discloses a contact structure comprising additional lines of contact in a surpline or staggered contact structure (Fig.2) instead of conventional single contact as shown in Fig.1A or Nojiri's Fig.6-7.

It would have been obvious to one of ordinary skill in the art to form the first and second interconnections in Nojiri's device with the contact structure as taught by Brintzinger in order to reduce potential of crack problem. See Brintzinger's col.3 lines 15-25.

So, the device being formed by the combination of Nojiri and Brintzinger inherently includes each of the interconnections comprises a plurality of individual contacts between the bond pad and the conductive islands and between the conductive islands and the active devices; the second interconnections comprise a relatively wide source contact layer and distributed connections to the power supply bus; the second interconnections comprise a relatively wide source contact layer and distributed connections to the power return bus; and the contacts between adjacent levels of the structure are distributed over the conductive islands.

Allowable Subject Matter

4. Claim 102 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance: above references do not teach that the contacts between a first pair of adjacent levels are laterally offset relative to the contacts between a second pair of adjacent levels. Prior art of record fails to teach or suggest to incorporate these limitations into above references to arrive at the claimed device.

Conclusion

6. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must

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conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

7. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

8. If attempts to reach the examiner by telephone are unsuccessful, the primary examiner Steven Loke who can be reached on (571) 272-1657.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.



Cuong Nguyen

Primary examiner

6/29/05